5-V Input, Variable Output, 20-A High-Efficiency Synchronous Buck Converter Using the UCC27223 with Predictive Gate Drive™ Technology

System Power

Contents

1 Introduction

The UCC27223EVM evaluation module (EVM) is a high efficiency, synchronous buck converter providing a variable output between 0.9 V and 1.8 V at up to 20 A from a 5-V input. The EVM is designed to start up from a single 5-V supply, and no additional bias voltage is required for start-up. The module uses the UCC27223 high-efficiency predictive synchronous buck driver with enable, along with the UCC3803 low-power BiCMOS current-mode PWM controller for demonstrating the Predictive Gate Drive™ (PGD) technique. Several advanced TI design and packaging technologies are used, providing the highest possible efficiency from step-down converters. Configured for voltage-mode control, UCC27223EVM operates at 500 kHz with a peak efficiency of 92% and a full load efficiency over 86% for V_{OUT} = 1.8 V.

The addition of the UCC27223's start-up and ENABLE features allow the EVM to start up the pre-biased supply or run in a low-power disabled mode by grounding a single pin. In this disabled mode, the EVM draws only 7 mA of current at 5 V and produces a floating output, allowing the pre-bias to return to the output and wait for the release of the ENABLE pin.

2 Description

The UCC27223 synchronous buck driver features the patented Predictive Gate Drive™ control technology to virtually eliminate body-diode conduction while also minimizing reverse recovery losses in synchronous rectifiers. This can result in significant improvements in synchronous rectifier switching efficiency over competing technologies such as adaptive delay control or fixed delay.

The UCC27223 3-A driver stage uses TI's unique TrueDrive™ technology hybrid Bipolar/CMOS output. The TrueDrive™ technology hybrid architecture consists of a mixed Bipolar/CMOS parallel output stage to take advantage of each technology's best features. Ultra-fast rise and fall times provide the highest possible drive current where it is needed most, at the MOSFET Miller plateau region and full rail to rail operation of the gate drive with very low V_{GS} impedance during turn-off for reduced dV/dt turn-on sensitivity.

The UCC27223 is available in TI's 14-pin PowerPAD™ package. PowerPAD™ is a thermally enhanced standard device package offering a three to five times improvement in power dissipation over similar standard device packages. With a junction-to-case thermal impedance of only 2°C/W, the UCC27223 typically requires no additional heatsink and operates at a much lower junction temperature resulting in increased component reliability.

The UCC27223EVM highlights the many benefits of using the UCC27223 high-efficiency predictive synchronous buck driver in conjunction with the UCC3803 low−power BiCMOS current-mode pwm controller. The following user guide provides the schematic, component list, assembly drawing, artwork and test set up necessary to evaluate the UCC27223 and UCC3803 in a typical synchronous buck application. The UCC27223EVM's pre-bias features allows the user to evaluate the UCC27223 in low voltage, pre-biased applications, such as multi-phase buck converters, ASIC and FPGAs with separate core and peripheral supply voltages.

2.1 Applications

The UCC27223EVM is designed for use in non-isolated 5-V input systems requiring high-efficiency and high-power density for very low-output voltage, high-current converter applications, including:

- Processor power
- General computer
- Datacom
- Telecom
- Point-of-load DC/DC conversion from intermediate bus voltage
- Multi-phase synchronous buck VRM

2.2 Features

- Up to 92% peak efficiency using the UCC27223 with Predictive Gate Drive™ technology
- 5-V typical input (4.5 V < V_{IN} < 5.5 V)
- 0.9-V to 1.8-V variable output allows PGD evaluation at most popular output voltages
- 20Adc output current for 0.9 V< V_{OUT} < 1.8 V
- High-frequency 500-kHz operation
- UCC3803 PWM control with low-voltage 4.1-V start up
- Compact size, low-profile, surface mount design (2.4” x 2.1” x 0.5”)
- Voltage-mode control
- Up to 90-kHz loop gain bandwidth for very fast transient response
- Double-sided PCB with power stage and devices all on top side
- Convenient scope jacks for probing predictive gate drive critical waveforms
- Diode isolated output pin available for pre-bias testing
- Enable/disable input available for external control circuit testing

3 UCC27223EVM Electrical Performance Specifications

The UCC27223EVM is variable to any output voltage between 0.9 V and 1.8 V. Within this range, some of the more common output voltages are 0.9 V, 1.2 V, 1.5 V and 1.8 V. Therefore, the electrical specifications for the UCC27223EVM were specifically derived at these voltage levels.

Table 1. Electrical Performance and Specifications

PARAMETER	CONDITIONS		V_{OUT}	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Voltage Range			All	4.75	5	5.5	V
Max Input Current	V_{IN} = 5 V,	I_{OUT} = 20 A	0.9		4.7	5.5	A
			1.2		5.9	7	
			1.5		7.2	8.6	
			1.8		8.4	10.0	
No−Load Input Current	V_{IN} = 5 V,	I_{OUT} = 0 A	0.9V		90	110	mA
			1.2V		95	115	
			1.5V		98	120	
			1.8V		100	120	
OUTPUT CHARACTERISTICS							
Output Voltage Set	V_{IN} = 5 V,	0 A< I_{OUT} < 20A	0.9V	0.89	0.90	0.91	V
			1.2V	1.19	1.20	1.22	
			1.5V	1.48	1.50	1.52	
			1.8V	1.78	1.80	1.82	
Line regulation	I_{OUT} = 0 A,	4.75 V< V_{IN} < 5.5 V	All			1%	
Load regulation	0 A < I_{OUT} < 20 A,	V_{IN} = 5 V	All			1%	
Output voltage ripple	V_{IN} = 5 V,	I_{OUT} = 20 A	0.9		20		$mV_{(p-p)}$
			1.2		26		
			1.5		31		
			1.8		36		
Output load current			All	0		20	A
Output overcurrent	Limit source current to 10 A Limit load current to 20 A				None		
Output current limit	Limit source current to 10 A Limit load current to 20 A				None		
CONTROL LOOP CHARACTERISTICS							
Switching frequency			All	450	500	550	kHz
Control loop bandwidth			All	60		100	kHz
Phase margin			All	30		60	°
EFFICIENCY							
Peak efficiency	V_{IN} = 5 V,	6 A < I_{OUT} < 10 A	0.9		86%		
			1.2		88%		
			1.5		90%		
			1.8		91%		
Full load efficiency	V_{IN} = 5 V,	I_{OUT} = 20 A	0.9		79%		
			1.2		81%		
			1.5		85%		
			1.8		86%		

4 Schematic

A schematic of the UCC27223EVM is shown in Figure 1. Terminal block J5 is the 5 V input voltage source connector and terminal block J7 is the output and return for the 0.9 V to 1.8 V variable output voltage.

U1 is the UCC27223 shown with all the necessary discrete circuitry for high efficiency operation. Q2 and Q3 are optimally selected based upon $R_{DS(on)}$, gate charge characteristics and input voltage requirements. In addition the synchronous rectifier, Q3 is chosen for dv/dt robustness. If the EVM is evaluated using Q2 and Q3 combinations different than originally configured, a small value (<10) of R8 may be required to control inadvertent dv/dt induced turn-on of Q3.

Scope jacks J2 and J3 allow the user to measure the gate drive signals into Q3, the synchronous rectifier MOSFET and Q2, the upper control MOSFET. J4 allows convenient access to the drain-to-source voltage of Q3, also known as the switch node. J1 allows probing of the UCC3803 output. With R4 removed, the UCC3803 output can be measured while disabling the input to the UCC27223, and effectively running the controller without the power stage.

The UCC3803 is a current-mode PWM controller configured for voltage-mode control for this application. The controller is stabilized over all specified line and load conditions, with the internal error amplifier configured using a type 3 compensation scheme. R14 provides a matched 50−Ω impedance for inserting a network analyzer between TP3 and TP4 for convenient, non-invasive measurement of the control loop.

The EVM can be set to regulate to output voltages between 0.9 V and 1.8 V by varying the resistance of the trim pot, R11. R10 is a fixed 11−kΩ resistor in series with R11, so that when R11 is set to 0 Ω, the correct amount of voltage added, due to R10, to the FB pin of U2 forces the output to regulate at 0.9 V. Conversely, when R11 is set to the maximum value (50 kΩ), and added to R10, the resulting voltage added to the FB pin of U2, forces the output voltage to regulate at 1.8 V.

The output inductor, L1 is a 0.6-μH, 22-A inductor and is commonly available from various manufacturers. However, due to the differences in component design, and specific winding techniques there can be a significant variance in the DC winding resistance from one manufacturers part to another. When designing for high-current output stages such as the UCC27223EVM, this can result in an efficiency gain or loss of as much as 1%. Therefore careful selection should be paid to properly select the optimal output inductor for a given synchronous buck application.

TP2 provides a convenient point to demonstrate the UCC27223's off−time until controlled start-up profile designed to minimize sink current through Q3 during start up and prevent the power stage from sinking current from a pre-biased supply. By applying a subregulation voltage to TP2, the start-up characteristics of the UCC27223 can be seen while D5 prevents voltage from flowing out TP2 and damaging the pre-bais test source, simulating an ESD protection diode present between different supply voltages on many FPGA and ASIC nodes.

TP1 provides easy, access to the UCC27223's ENABLE pin (U1 pin 2) for external control of the UCC27223's enable feature. The pin is active high and powered by the internal pull-up resistor of the UCC27223. Grounding TP1 forces both G1 and G2 outputs of the UCC27223 to their low impedance states, holding both Q2 and Q3 in their OFF state.

R16 provides a small output load (1.0 kΩ) to sink current supplied by the feedback circuit while the output is disabled. If a more typical ground referenced feedback circuit is used, or a minimum 2-mA load is presented to the output, this additional load is not necessary when the driver is disabled. With no load on the output, current from V_{REF} forces the output to rise and shut down the UCC3803 controller.

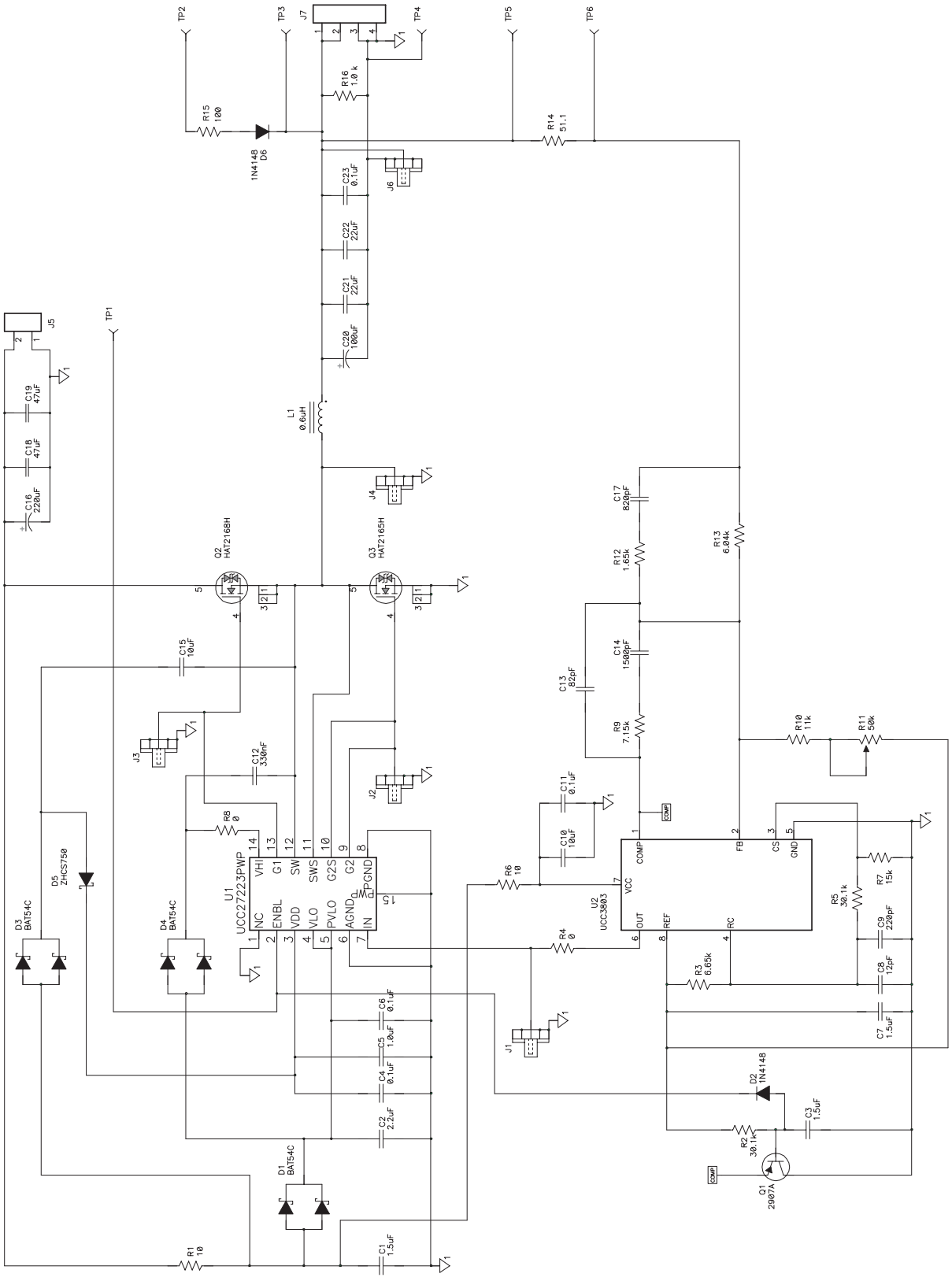


Figure 1. UCC27223EVM Schematic

Q1, R2 and C3 provide a simple soft start circuit, restricting V_{COMP} to U2 (UCC2803) during start-up. D2 forces the circuit to go back through start-up when ENABLE is grounded and then released. This prevents the controller from going to maximum duty cycle while the driver is disabled, and overshooting when the drive is released. R2 and C3 have been selected to provide a sloped soft start profile, and minimize any current loading on a pre−bias supplied to TP2 (BIAS) during start-up or disable recovery.

5 Variable Output Voltage

The output voltage of the UCC27223EVM is variable between 0.9 V and 1.8 V, over the full range of the V_{OUT}-Adjust potentiometer, R11. By turning the V_{OUT}-Adjust knob all the way clockwise, the output voltage regulates at 1.8 V. Or, by rotating the V_{OUT}-Adjust knob completely counterclockwise, the output voltage regulates at 0.9 V. Intermediate voltages can be dialed in, by rotating the V_{OUT}-Adjust knob and monitoring the output voltage accordingly. Due to the 10% tolerance of the potentiometer, it may not be possible, in some cases, to get exactly 1.800 V, or 0.900 V. Figure 2 shows graphically how V_{OUT} varies as a function of the resistance of R11, making it simple to replace R11 with a fixed resistor for a given fixed output voltage.

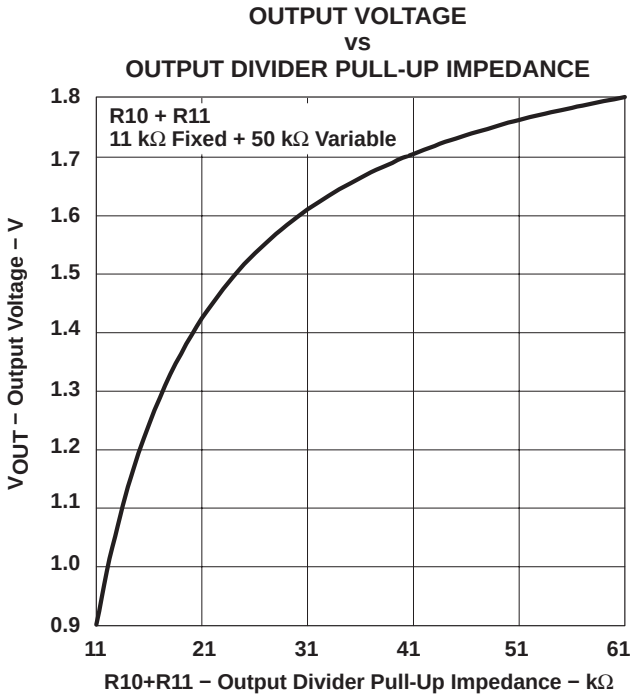


Figure 2.

CAUTION:

Output voltage should be varied only while V_{IN} is with the limits specified in Table 1, and I_{OUT} is 0 A_{DC}. High currents flowing between the source voltage and the EVM, and between the output load and the EVM result in significant voltage drops through these connections. Varying the output voltage under heavy load can cause the input voltage to fall out of spec during maximum load current.

6 Test Set Up

Figure 3 shows is the basic test set up recommended to evaluate the UCC27223EVM. Please note that although the return for J5 is the same as the J7 return, the V_{IN} and LOAD1 connections should remain separate as shown below.

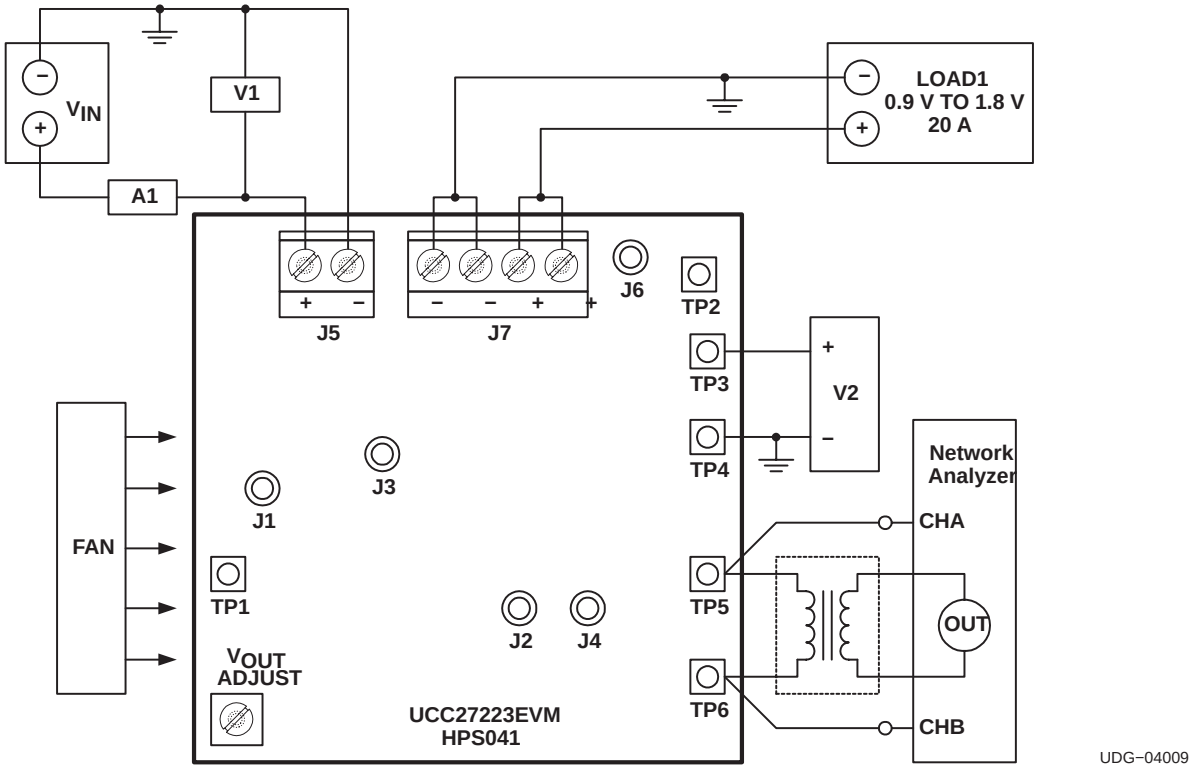


Figure 3. Recommended EVM Test Configuration

6.1 Ouptut Load (LOAD1)

For the output load to V_{OUT}, use a programmable electronic load set to constant current mode and capable of sinking 0 A_{DC} to 20A_{DC}. Using a dc voltmeter, V2, it is also advised to make all output voltage measurements directly at TP3 and TP4 terminals. Measuring V_{OUT} at LOAD1 or J7 results in some voltage measurement error, especially at higher load current, due to finite voltage drops across J7 and the wires between J7 and the electronic load.

CAUTION:

The UCC27223EVM does not provide output overcurrent protection. In order to avoid possible damage to the EVM, it is recommended to limit the maximum load current to 20 A_{DC}.

6.2 DC Input Source (V_{IN})

The input voltage should be a variable DC source capable of supplying between 0 Vdc and 6 Vdc at no less than 10 Adc, and connected to J5 as shown in Figure 3. For fault protection to the EVM, good common practice is to limit the source current to no more then 9 A_{DC} for a 5-V input. A dc ammeter, A1 should also be inserted between V_{IN} and J5 as shown in Figure 2.

6.3 Network Analyzer

A network analyzer can be connected directly to TP5 and TP6 as shown in Figure 3. The UCC27223EVM provides a 51.1-Ω resistor (R14) between the output and the voltage feedback to allow easy non-invasive measurement of the control to output loop response.

6.4 Recommended Wire Gauge

The connection between the source voltage, VIN and J5 of the EVM can carry as much as 10 A_{DC}. The minimum recommended wire size is AWG #18 with the total length of wire less than 8 feet (4 feet input, 4 feet return). The connection between J7 of the EVM and LOAD1 can carry as much as 20 A_{DC}. The minimum recommended wire size is AWG #16, with the total length of wire less than 8 feet (4 feet output, 4 feet return). Due to the low output voltage, and the limitations of an electronic load, larger wire with shorter total length may be required.

6.5 Oscilloscope Probe Test Jacks

J1, J2, J3, J4 and J6 are available to allow accurate probing and measuring of high speed noise sensitive signals such as gate drive voltage, switch-node voltage and output voltage ripple. The measurements that must be made to understand Predictive Gate Drive™ technology involve waveforms that are dithering within a 10-ns window. Using the pigtail ground lead commonly found on most oscilloscope probes results in unreliable measurements.

6.6 Fan

Most power converters include components that can get hot to the touch when approaching temperatures of 60°C. Because this EVM is not enclosed to allow probing of circuit nodes, a small fan capable of 200−400 LFM is recommended to reduce component temperatures when operating the EVM.

7 Power Up/ Power Down Test Procedure

The following test procedure is recommended primarily for power up and shutting down the EVM. Whenever the EVM is running above an output load of 10 A_{DC}, the fan should be turned on. Also, never walk away from a powered EVM for extended periods of time.

1. Working at an ESD workstation, make sure that any wrist straps, boot straps or mats are connected referencing the user to earth ground before power is applied to the EVM. Electrostatic smock and safety glasses should also be worn.
2. Prior to connecting the DC input source, V_{IN}, it is advisable to limit the source current from V_{IN} to a 9-A maximum. Connect the ammeter A1 (0-A to 10-A range) between V_{IN} and J5 as shown in Figure 3. Make sure V_{IN} is initially set to 0 V.
3. Connect LOAD1 to J7 as shown in Figure 3. Set LOAD1 to constant current mode to sink 0 A_{DC} before V_{IN} is applied.
4. Connect the voltmeter, V2 to TP3 and TP4 as shown in Figure 3.
5. Increase V_{IN} from 0 V to 5 V_{DC}, while monitoring the output voltage on V2. V_{OUT} should be in regulation when V_{IN} > 4.5 V.

6. Vary LOAD1 anywhere between 0 A to 20 A_{DC}, making sure to turn on fan blowing air directly on the EVM for loads above 10 A.
7. Vary the input voltage between 4.5 V and 5.5 V.
8. Vary the V_{OUT}-Adjust over the full range to verify that the output voltage changes accordingly.
9. Shut down the electronic load.
10. Shut down V_{IN}.

8 Predictive Gate Drive™ Technology

8.1 Expected Efficiency Improvement with the UCC27223EVM

The benefits of Predictive Gate Drive™ technology become more significant at higher frequency and lower output voltage. For a synchronous buck converter, operating under similar specifications as shown in Table 1, but not employing Predictive Gate Drive™ technolgy, a total synchronous rectifier body-diode conduction time of as much as 120 ns can exist. Due to the reduction in body-diode conduction time, the UCC27223EVM demonstrates a significant savings in the amount of power dissipated in the synchronous rectifier, Q3.

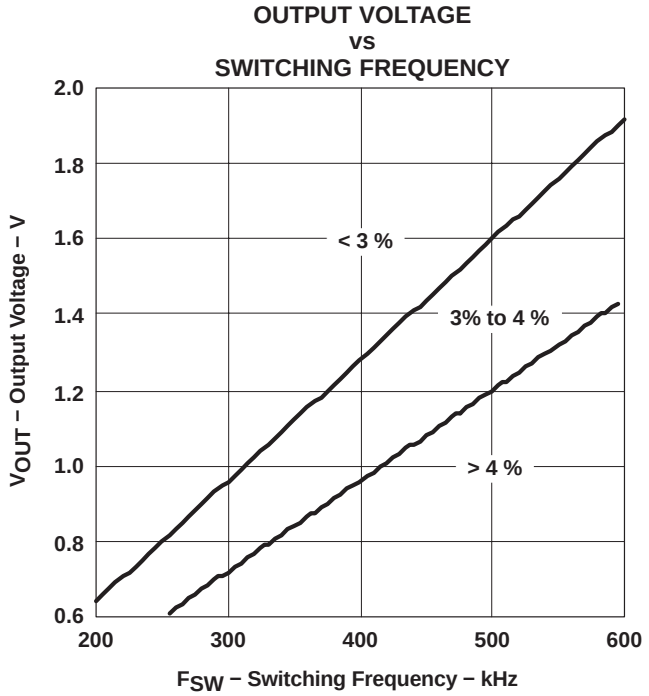


Figure 4.

In terms of overall efficiency gain, the graph shown in Figure 4 summarizes the amount of benefit that can be expected from the UCC27223EVM with Predictive Gate Drive™ control, compared to a similar design not using Predictive Gate Drive™ control technology. The UCC27223EVM operates at 500 kHz. Referring to Figure 4, at 500 kHz, when the output voltage of the UCC27223EVM is adjusted to less than 1.2 V, a 4% increase in overall converter efficiency can be expected. Similarly, a 3% to 4% increase can be expected for 1.2 V < V_{OUT}<1.6 V, and an increase of slightly less than 3% is typical for 1.6 V < V_{OUT} < 1.8 V.

8.2 Predictive Gate Drive™ In Action

All waveforms shown in Figures 5 through 8, were recorded with V_{IN} = 5 V, V_{OUT} = 1.8 V and I_{OUT} = 20A. Using Tektronix P6138 or equivalent oscilloscope probes, inserted into J2 and J3 (as seen in Figure 2), the complementary gate drive signals of Q2 and Q3 are shown in Figure 5. Extremely fast rise and fall times as well as the minimal near zero delay between Q3 turn-off and Q2 turn-on should also be noted. Some dithering on the rising edge of Q2 and Q3 can be observed. A characteristic of Predictive Gate Drive™ technolgy, dithering should be nearly constant and limited to within a 10 ns window during the time that body-diode conduction would be occurring in Q3.

J4 shown in Figure 3 allows convenient probing of the switch-node voltage, shown in Figure 6. The ringing shown on the switch-node voltage waveform is a result of component package inductance and parasitic inductance between the UCC27223 driver device and the high-speed switching MOSFETs, and is not a characteristic of Predictive Gate Drive™ technolgy. Predictive Gate Drive™ technolgy minimizes body-diode conduction as highlighted at points A and B of Figure 6. Figure 7 and Figure 8 show close up views of points A and B shown in Figure 6. Figure 8 shows some inductive ringing below the ground reference; however, it is not clamped by the body-diode of Q3.

9 Performance Data and Characteristic Curves

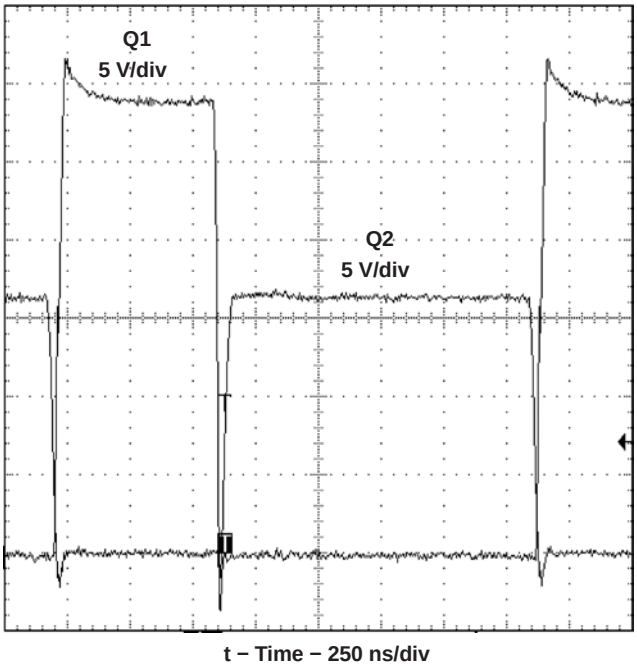


Figure 5. Complementary Gate Drive Voltage

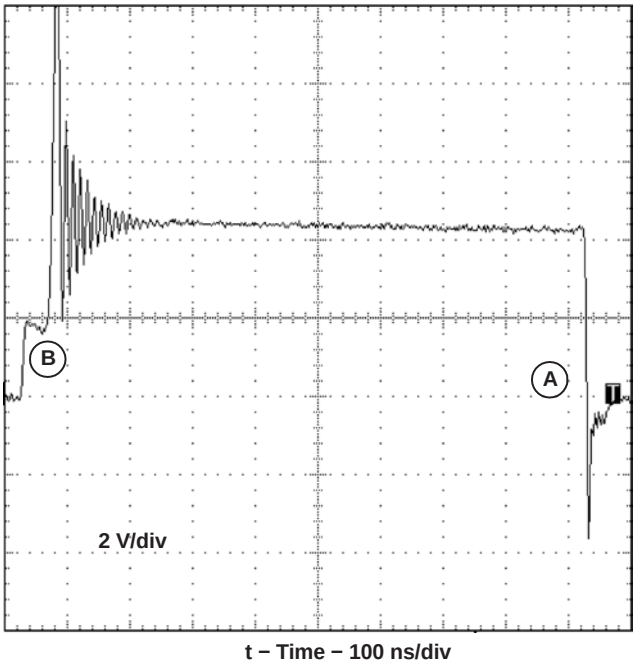
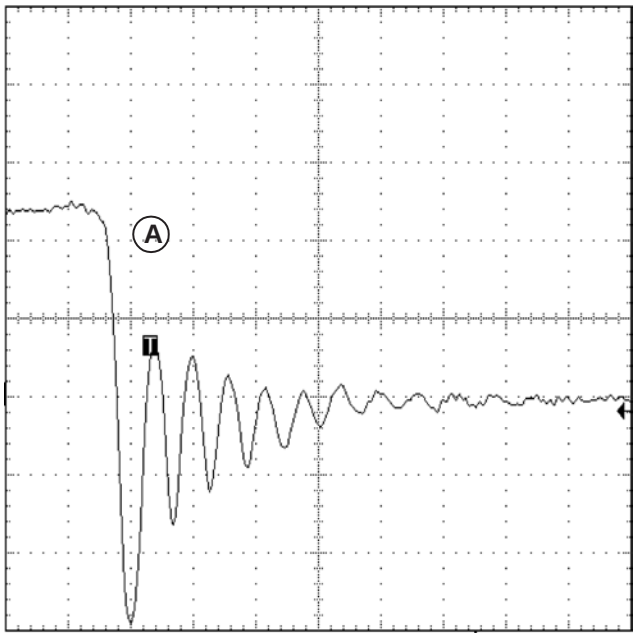
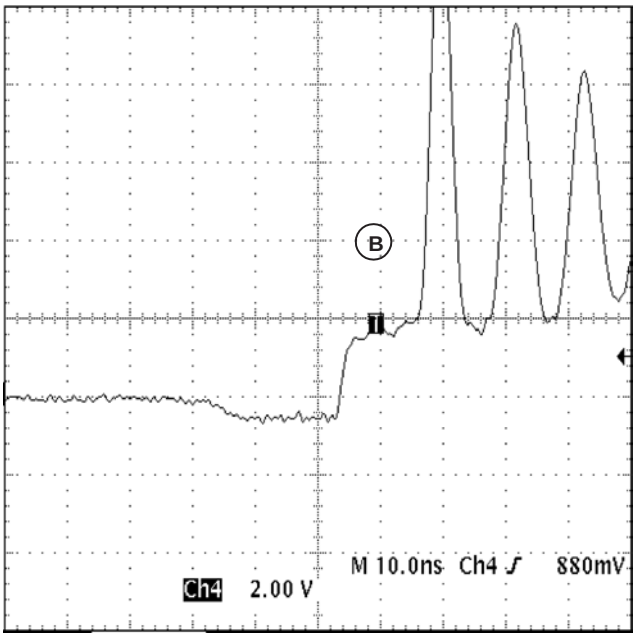


Figure 6. Switch-Node Voltage



t − Time − 10 ns/div

Figure 7. Close Up: Switch-Node A



t − Time − 10 ns/div

Figure 8. Close Up: Switch-Node B

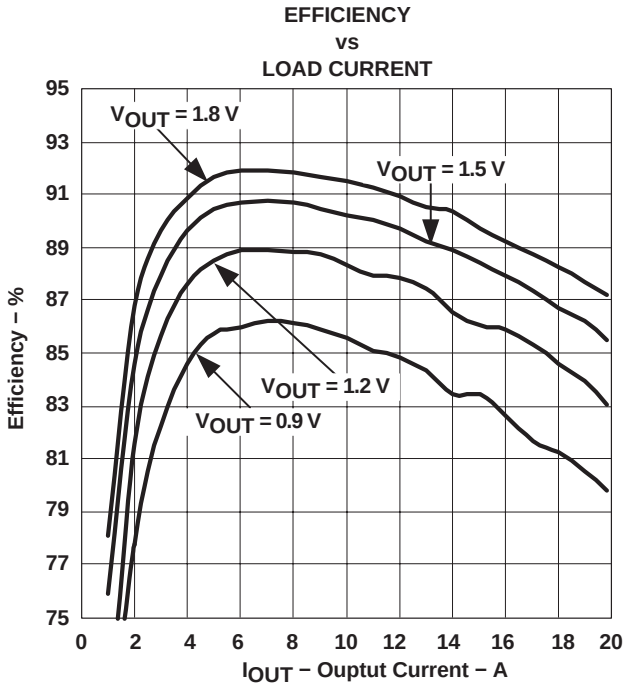


Figure 9.

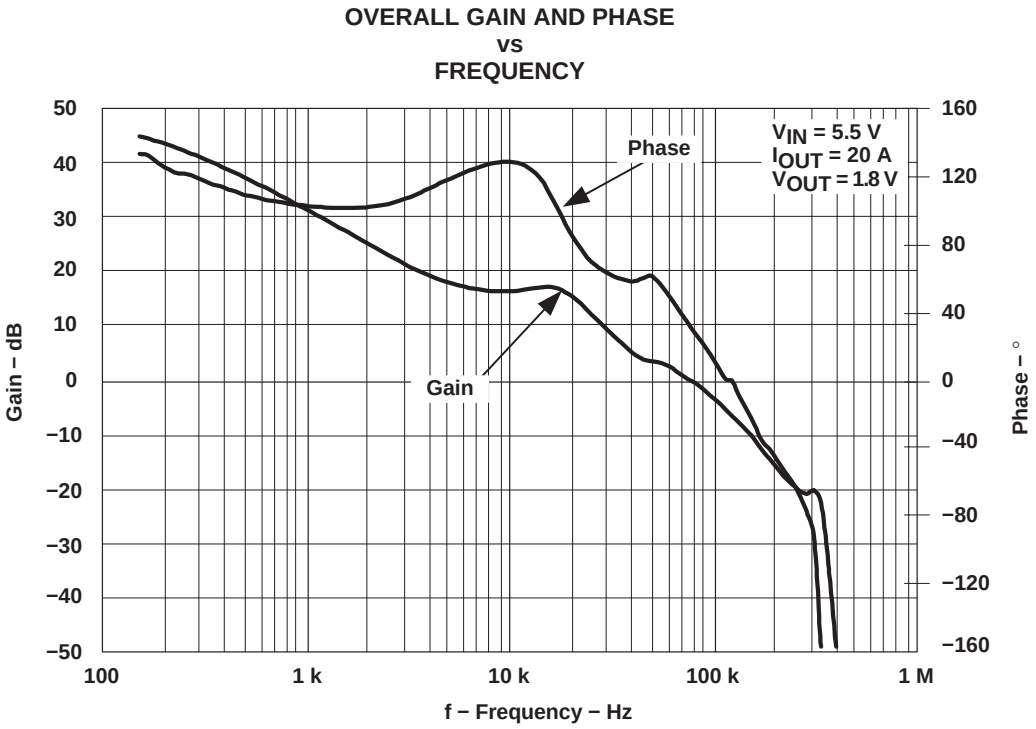


Figure 10.

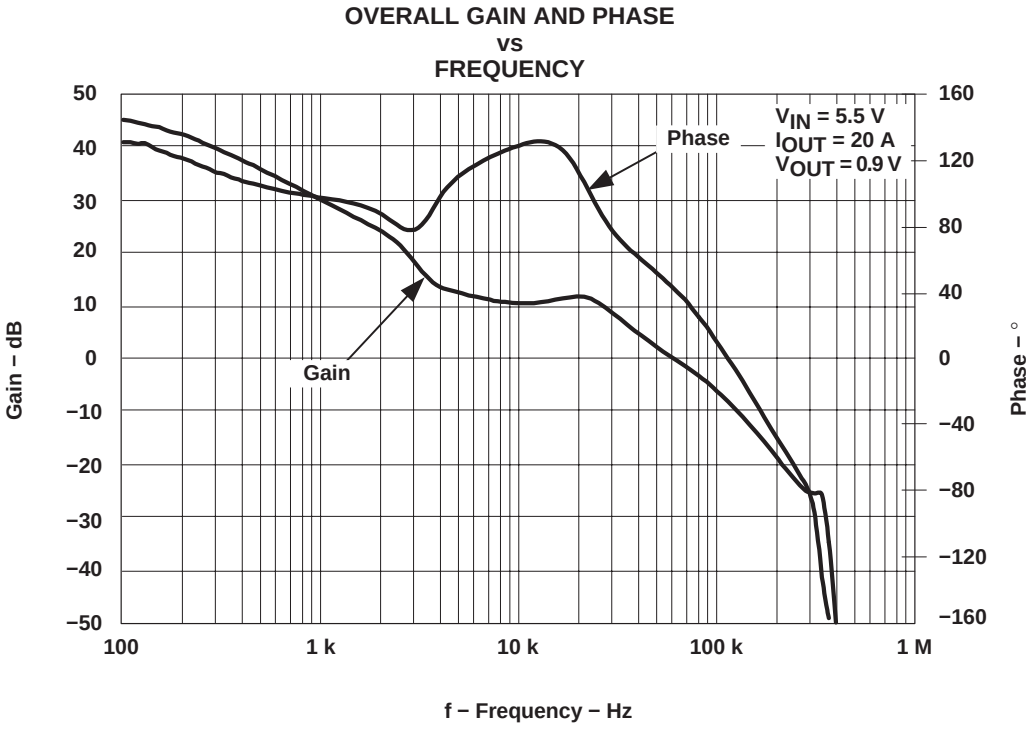
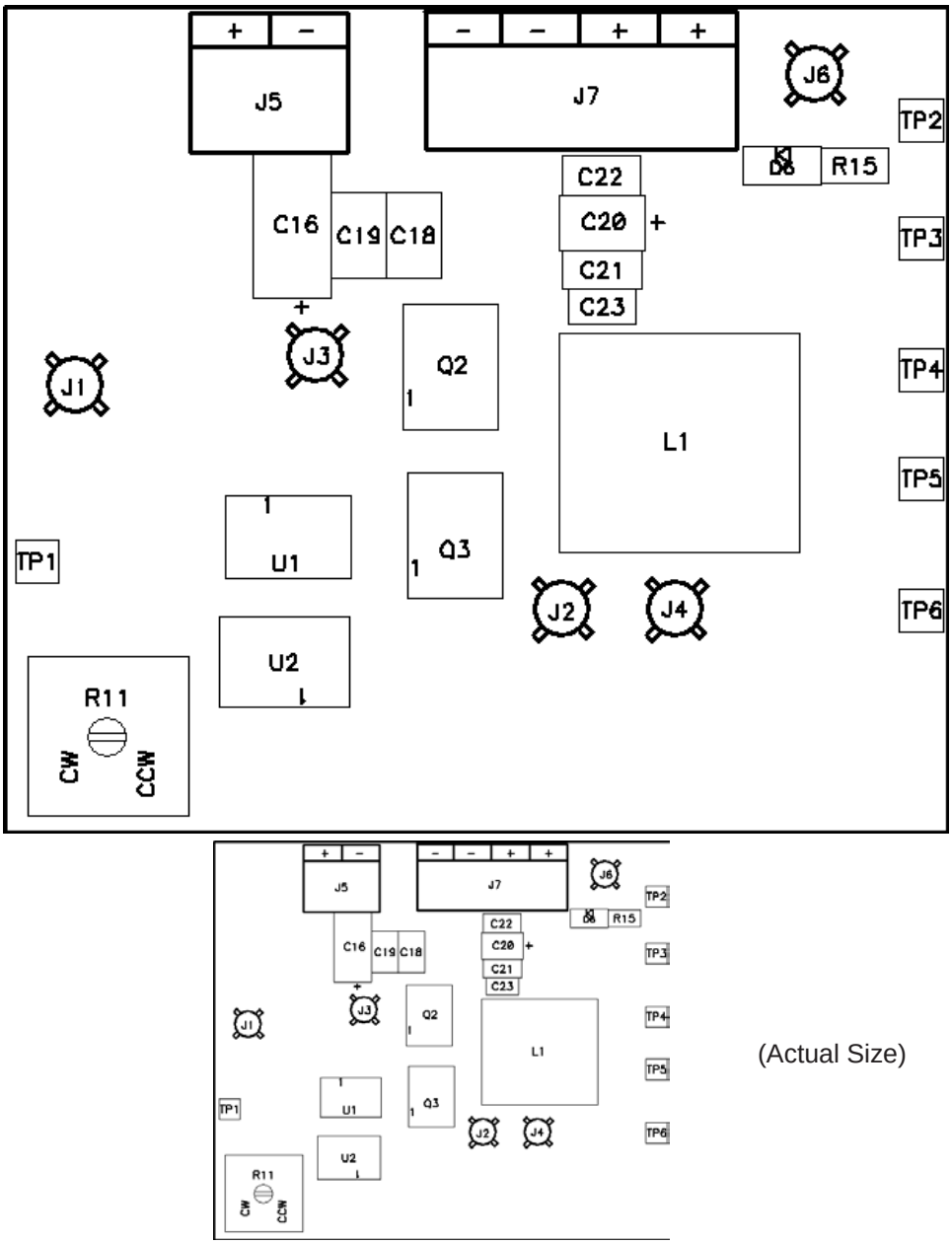


Figure 11.

10 EVM Assembly Drawing and Layout

Figures 12 and 17 show the top and bottom-side component placement for the EVM, as well as device pin 1 designators where necessary. A four layer PCB was designed with the power stage on the top layer with the support and signal components on the bottom layer. The ground return path on the bottom layer and internal layers has been designed to keep power return current isolated from the low level analog signals and minimize ground loop inductance. The PCB dimensions are 2.1” x 2.4” with a design goal of maintaining all components to less than 0.5” high measured between the top and bottom layers. All components are standard OTS surface mount components placed on the both sides of the PCB. The copper-etch for each layer is also shown.



(Actual Size)

Figure 12. Top Side Component Assembly

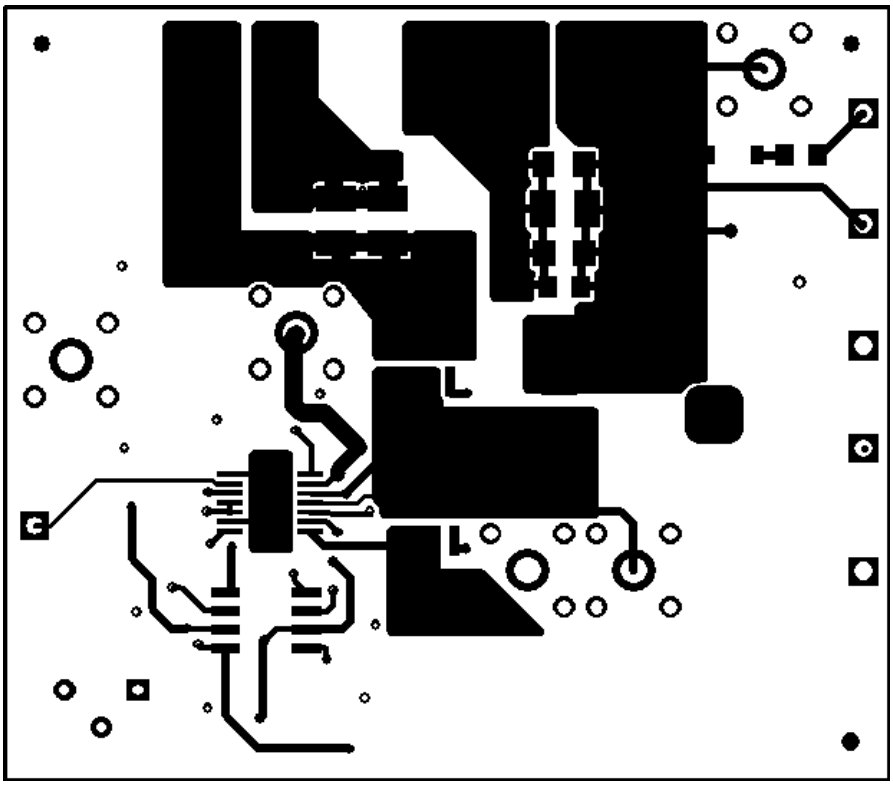


Figure 13. Top Signal Trace Layer

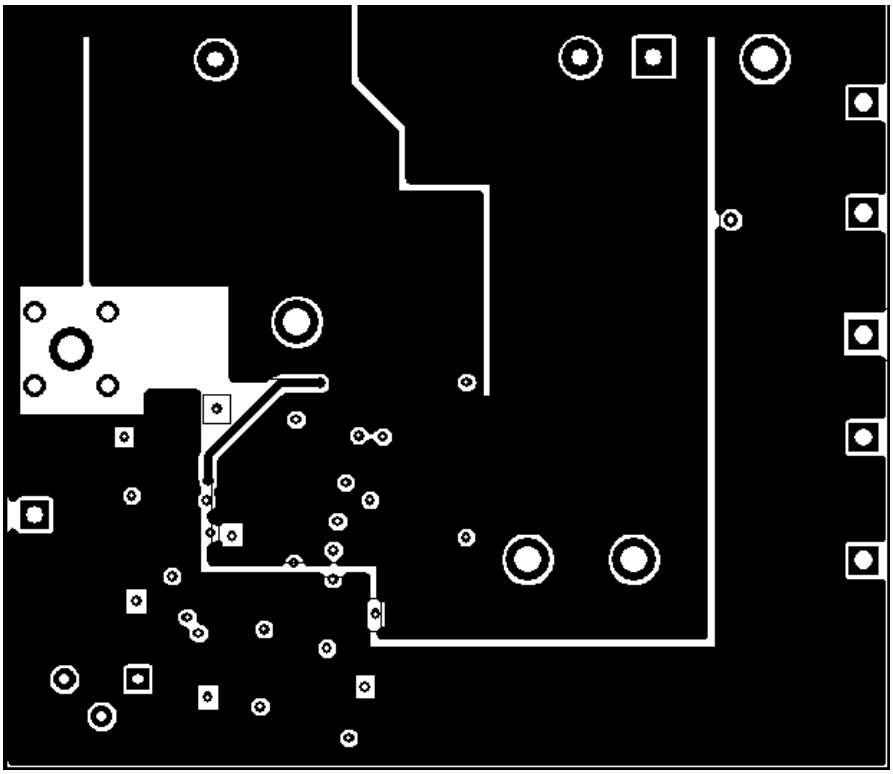


Figure 14. Internal Ground Plane

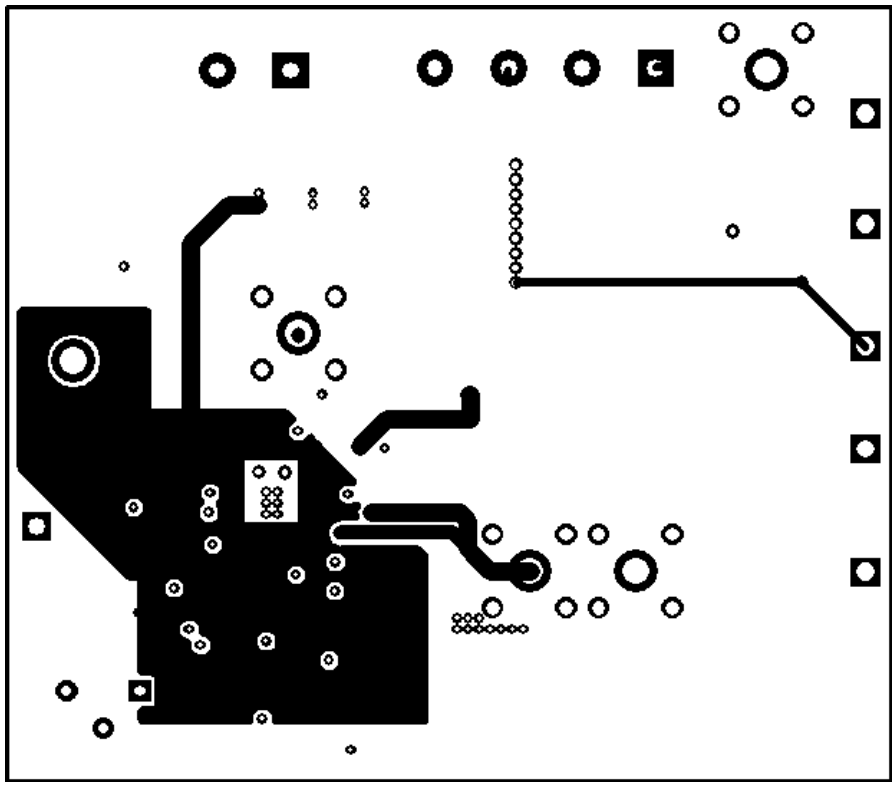


Figure 15. Internal Signal Ground and Trace Layer

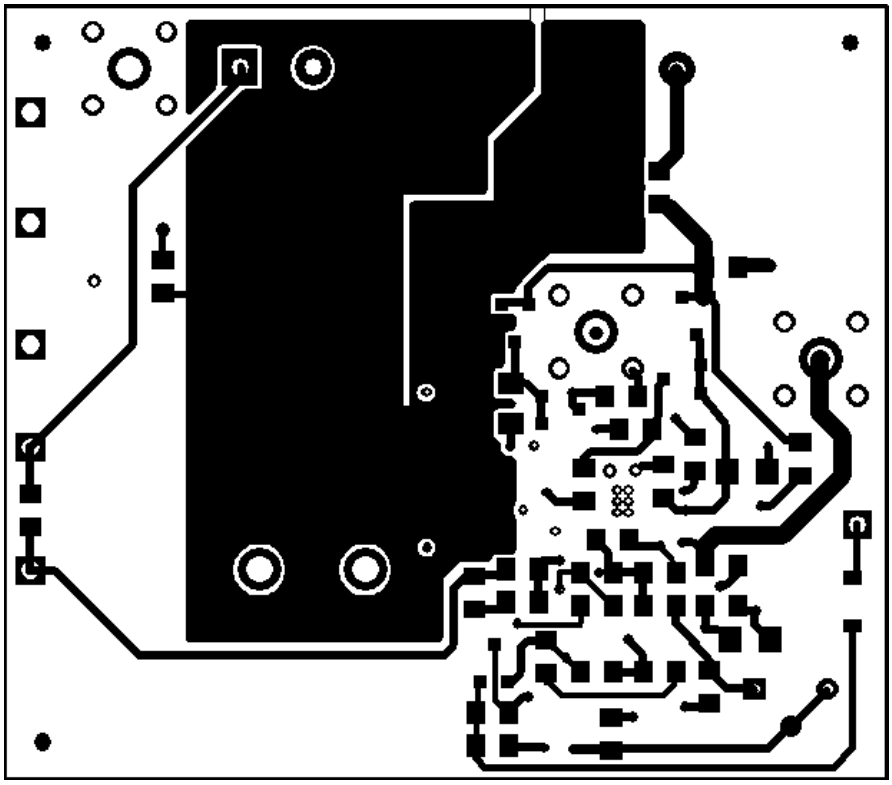


Figure 16. Bottom Signal Trace Layer (viewed from bottom)

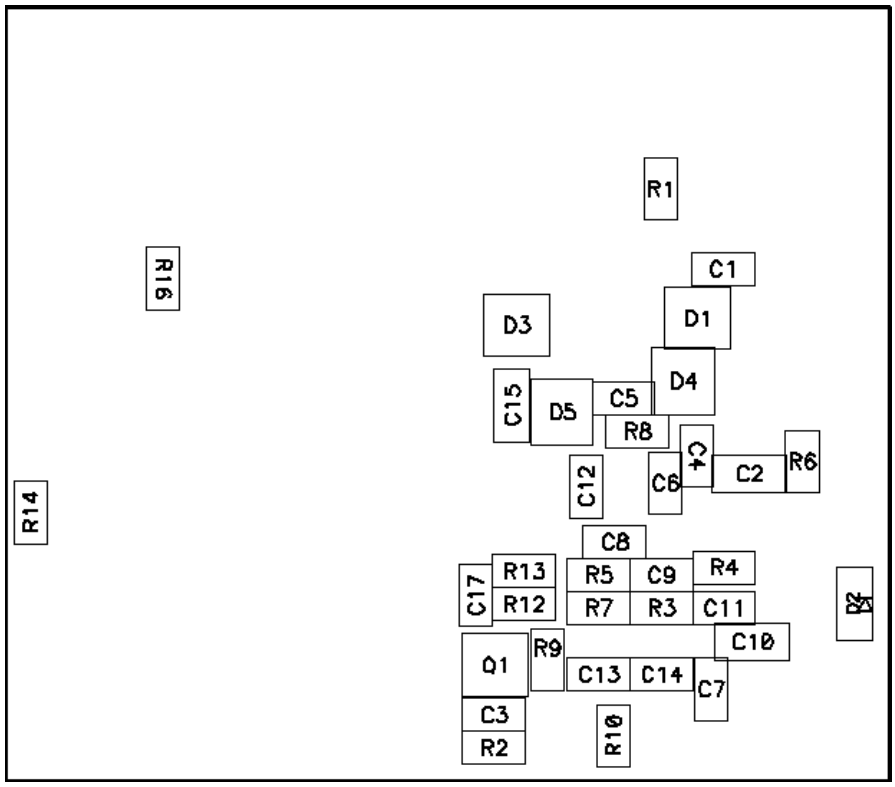


Figure 17. Bottom Side Component Assembly (viewed from bottom)

11 List of Materials

Table 2 lists the EVM components as configured according to the schematic shown in Figure 1.

Table 2. UCC27223EVM List of Materials

REFERENCE DESIGNATOR	QTY	DESCRIPTION	MFR	PART NUMBER
C1, C3, C7	3	Capacitor, ceramic, 1.5 µF, 10 V, X5R, 20%	TDK	C2012X5R1A155M
C2	1	Capacitor, ceramic, 2.2 µF, 25 V, X7R, 10%	TDK	C3216X7R1E225K
C4, C6, C11, C23	4	Capacitor, ceramic, 0.1 µF, 25 V, X7R, 20%	Std	Std
C5	1	Capacitor, ceramic, 0.1 µF, 16 V, X7R, 20%	TDK	C2012X7R1C105M
C8	1	Capacitor, ceramic, 12 pF, 50 V, NPO, 5%	Std	Std
C9	1	Capacitor, ceramic, 220 pF, 50 V, NPO, 5%	Std	Std
C10, C15	2	Capacitor, ceramic, 10 µF, 10 V, X5R, 20%	TDK	C3216X5R1A106M
C12	1	Capacitor, ceramic, 330 pF, 50 V, NPO, 5%	Std	Std
C13	1	Capacitor, ceramic, 82 pF, 50 V, NPO, 5%	Std	Std
C14	1	Capacitor, ceramic, 1500−pF, 50 V, NPO, 5%	Std	Std
C16	1	Capacitor, POSCAP, 220 µF, 6.3 V, 40 mΩ, 20%	Sanyo	6TPB220ML
C17	1	Capacitor, ceramic, 820 pF, 50 V, NPO, 5%	Std	Std
C18, C19	2	Capacitor, ceramic, 47 µF, 6.3 V, X5R, 20%	TDK	C3225X5R0J476M
C20	1	Capacitor, POSCAP, 100 µF, 4 V, 70 mΩ, 20%	Sanyo	4TPB100M
C21, C22	2	Capacitor, ceramic, 22 µF, 6.3 V, X7R, 20%	TDK	C3216X5R0J226M

REFERENCE DESIGNATOR	QTY	DESCRIPTION	MFR	PART NUMBER
D1, D3, D4	3	Diode, dual Schottky, 200 mA, 30 V, mΩ	Vishay	BAT54C
D2, D6	2	Diode, dual Schottky, 300 mA, 75 V, 30	Vishay	1N4148W
D5	1	Diode, Schottky, 750 mA, 40 V	Zetex	ZHCS750
J1, J2, J3, J4, J6	5	Adaptor, 3.5 mm probe clip (or 131−5031−00)	Tektronix	131−4244−00
J5	1	Terminal block, 2 pin, 15 A, 5.1 mm	OST	ED500/2DS
J7	1	Terminal block, 4 pin, 15 A, 5.1 mm	OST	ED500/4DS
L1	1	Inductor, SMT, 0.6 μH, 22−A, 0.6 mΩ	Pulse	PG0006.601
Q1	1	Bipolar, PNP, 60 V, 600 mA	Vishay	MMBT2907A
Q2	1	MOSFET, N-channel, 30 V, 30 A, 6 mΩ	Renesas (Hitachi)	HAT2168H
Q3	1	MOSFET, N-channel, 30−V, 55 A, 2.5 mΩ	Renesas (Hitachi)	HAT2165H
R1, R6	2	Resistor, chip, 10 Ω, 1/10 W, 1%	Std	Std
R2	1	Resistor, chip, 1M Ω, 1/10 W, 1%	Std	Std
R3	1	Resistor, chip, 6.65 kΩ, 1/10 W, 1%	Std	Std
R4, R8	2	Resistor, chip, 0 Ω	Std	Std
R5	1	Resistor, chip, 30.1 kΩ, 1/10 W, 1%	Std	Std
R7	1	Resistor, chip, 15 kΩ, 1/10 W, 1%	Std	Std
R9	1	Resistor, chip, 7.15 kΩ, 1/10 W, 1%	Std	Std
R10	1	Resistor, chip, 11 kΩ, 1/10 W, 1%	Std	Std
R11	1	Resistor, trim potentiometer, 50 kΩ, 10%	Bourns	3386P−1−503T
R12	1	Resistor, chip, 1.65 kΩ, 1/10 W, 1%	Std	Std
R13	1	Resistor, chip, 6.04 kΩ, 1/10 W, 1%	Std	Std
R14	1	Resistor, chip, 51.1 Ω, 1/10 W, 1%	Std	Std
R15	1	Resistor, chip, 100 Ω, 1/10 W, 1%	Std	Std
R16	1	Resistor, chip, 1.0 kΩ, 1/10 W, 1%	Std	Std
TP1, TP2, TP3, TP4, TP5, TP6	6	PCB pin, 0.043 hole, 0.3 Length	Mill−Max	3103-1-00-15-00-00-0X-0
U1	1	IC, predictive synchronous buck driver	TI	UCC27223PWP
U2	1	IC, low-power BiCMOS current-mode PWM	TI	UCC3803D
	1	PCB, FR4, 2.4” x 2.1” x 0.062”	Any	HPA041
	4	Bumpon, transparent, 0.44” x 0.2”	3M	SJ5303

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265